



THE **IIPC**  
HUSTLE AND GLORY



# NATIONWIDE ROADSHOW ON DIGITAL INDIA RISC-V VEGA PROCESSORS

Unleashing the Power of VEGA: Igniting Innovation Across India

**NOVEMBER 17 - 18, 2023**

## Venue

Guru Tegh Bahadur Institute of Technology  
G-8 Area, Rajouri Garden, New Delhi-110064

## Registration Fee - NIL

<https://vegaprocessors.in/dirv-roadshow2023/>



संयुक्त प्रशासन  
संयुक्त प्रशासन  
MINISTRY OF  
ELECTRONICS AND  
INFORMATION TECHNOLOGY

**VEGA**  
PROCESSOR

**IEEE** INDIA  
COUNCIL





## GTBIT at a Glance

Guru Tegh Bahadur Institute of Technology (GTBIT) was established in 1999 by Delhi Sikh Gurdwara Management Committee (DSGMC), which is running a host of educational institutes, besides carrying out large number of religious & social activities. GTBIT is a degree level technical institute, approved by AICTE and affiliated to Guru Gobind Singh Indraprastha University, Delhi. GGSIPU was established by Government of NCT of Delhi under provisions of Guru Gobind Singh University Act, 1998 read with its Amendment in 1999. It is an affiliating and teaching University. It is recognised by University Grant Commission, India under section 12B of UGC Act. It has also been accredited "A Grade" by NAAC. GTBIT has a sprawling campus & is centrally located in Rajouri Garden, New Delhi. The institute has five spacious buildings and state-of-the-art laboratories. Students of GTBIT have the best of facilities, conducive environment for studies & dedicated faculty to guide them and lead them to success.

## IIPC-GTBIT AND IEEE-GTBIT

**Industry Institute partnership cell (IIPC)** is established for enhancing the relationship between the institute and industry. This cell identifies the industrial expectation and promotes institutional preparation for meeting industrial needs by facilitating sponsored R&D projects, seminars, workshops and various other industrial training programmes. Organising such IIPC's in institution makes an effective contribution to educational system rather than criticizing shortcomings which are expected by the industry.

The **IEEE GTBIT Student Branch** was set up in the year 2008 with an aim to enhance the engineering skills of students in GTBIT. The student branch has been actively involved in achieving these goals and fostering leadership values not just among its members, but also the non-members of college. The growth of IEEE education programs is to ensure the growth of skill and knowledge in the technical professions and to foster individual commitment to continuing education among IEEE members.







## ABOUT THE EVENT

The DIR-V VEGA nationwide roadshow, jointly organized by IEEE India Council and C-DAC, MeitY, will be held concurrently at various centers across India. This comprehensive training program, encompassing hands-on sessions, offers a deep dive into the VEGA series of processors and ecosystem. The training covers both theoretical foundations and practical applications, including insights into ARIES development boards, SDK and application development. Experts from C-DAC, integral members of the VEGA Processor development team, will deliver the training sessions. This workshop is designed for a diverse audience, including students, faculty members, research scholars, and industry professionals. Certificates will be awarded upon successful completion of the workshop.

## DIR-V VEGA MICROPROCESSOR

DIR-V VEGA Microprocessors is a series of indigenous microprocessors developed by C-DAC, MeitY, Govt. of India under the Digital India RISC-V (DIR-V) program. The VEGA series comprises of 32/64-bit Single/Dual/Quad Core superscalar Out-of-Order high performance processors based on RISC-V Instruction Set Architecture. The first VEGA processor based SoC chip THEJAS32, a 32-bit Single core SoC has been successfully fabricated. A fully indigenous and "Made in India" ARIES development platform based on THEJAS32 chip has been made widely available, targeted for both industry and academia involving embedded system design and IoT applications.

## 15 REGIONAL CENTRES ACROSS THE COUNTRY





## IMPORTANT DATES

Last Date for Participants to Register for workshop:	25th October 2023
Announcement of the First List of Participants:	27th October 2023
Last date for Paying Registration Fee:	30th October 2023
Announcement of the Second List of Participants:	31st October 2023
Last date for Paying Registration Fee:	3rd November 2023
Nationwide VEGA Workshop at Regional Venues	17th November - 18th November 2023
Certificate Distribution to Participants:	30th November 2023

## ORGANIZING TEAM

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 @VEGAProcessors  
 @VegaProcessor

Every participant of the two-day workshop during the roadshow will receive a certificate from IEEE India Council and C-DAC





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For more details & registration  
kindly visit the roadshow website

<https://vegaprocessors.in/dirv-roadshow2023/>

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