GURU Tegh Bahadur Institute of Technology(ECE Deptt.)

Subject: DSD(Digital System Design) Semester:5th

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1)   The utilization of CAD tools for drawing timing waveform diagram and transforming it into a network of logic gates is known as \_\_\_\_\_\_\_\_.

**a. Waveform Editor  
b. Waveform Estimator  
c. Waveform Simulator  
d. Waveform Evaluator**

**ANSWER: Waveform Editor**

**2)   Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?**

**a. Simulation  
b. Optimization  
c. Synthesis  
d. Verification**

**ANSWER: Synthesis**

**3)   Among the VHDL features, which language statements are executed at the same time in parallel flow?**

**a. Concurrent  
b. Sequential  
c. Net-list  
d. Test-bench**

**ANSWER: Concurrent**

**4)   In Net-list language, the net-list is generated \_\_\_\_\_\_\_synthesizing VHDL code.**

**a. Before  
b. At the time of (during)  
c. After  
d. None of the above**

**ANSWER: After**

**5)   In VHDL, which object/s is/are used to connect entities together for the model formation?**

**a. Constant  
b. Variable  
c. Signal  
d. All of the above**

**ANSWER: Signal**

**6)   Which data type in VHDL is non synthesizable & allows the designer to model the objects of dynamic nature?**

**a. Scalar  
b. Access  
c. Composite  
d. File**

**ANSWER: Access**

**7)   Which type of simulation mode is used to check the timing performance of a design?**

**a. Behavioural  
b. Switch-level  
c. Transistor-level  
d. Gate-level**

**ANSWER: Gate-level**

**8)   In the simulation process, which step specifies the conversion of VHDL intermediate code so that it can be used by the simulator?**

**a. Compilation  
b. Elaboration  
c. Initialization  
d. Execution**

**ANSWER: Elaboration**

**9)   Which type of simulator/s neglect/s the intra-cycle state transitions by checking the status of target signals periodically irrespective of any events?**

**a. Event-driven Simulator  
b. Cycle-based Simulator  
c. Both a and b  
d. None of the above**

**ANSWER: Cycle-based Simulator**

**10)   Which among the following is not a characteristic of ‘Event-driven Simulator’?**

**a. Identification of timing violations  
b. Storage of state values & time information  
c. Time delay calculation  
d. No event scheduling**

**ANSWER: No event scheduling**

**11)   Which among the following is an output generated by synthesis process?**

**a. Attributes & Library  
b. RTL VHDL description  
c. Circuit constraints  
d. Gate-level net list**

**ANSWER: Gate-level net list**

**12)   Register transfer level description specifies all of the registers in a design & \_\_\_\_\_\_ logic between them.**

**a. Sequential  
b. Combinational  
c. Both a and b  
d. None of the above**

**ANSWER: Combinational**

**13)   Which type of digital systems exhibit the necessity for the existence of at least one feedback path from output to input?**

**a. Combinational System  
b. Sequential system  
c. Both a and b  
d. None of the above**

**ANSWER: Sequential system**

**14)   The output of sequential circuit is regarded as a function of time sequence of \_\_\_\_\_\_\_\_\_\_.  
A. Inputs  
B. Outputs  
C. Internal States  
D. External States**

**a. A & D  
b. A & C  
c. B & D  
d. B & C**

**ANSWER: A & C**

**15)   The time required for an input data to settle \_\_\_\_\_ the triggering edge of clock is known as ‘Setup Time’.**

**a. Before  
b. During  
c. After  
d. All of the above**

**ANSWER: Before**

**16)   Hold time is defined as the time required for the data to \_\_\_\_\_\_\_\_ after the triggering edge of clock.**

**a. Increase  
b. Decrease  
c. Remain stable  
d. All of the above**

**ANSWER: Remain stable**

**17)   In VHDL, which class of scalar data type represents the values necessary for a specific operation?**

**a. Integer types  
b. Real types  
c. Physical types  
d. Enumerated types**

**ANSWER: Enumerated types**

**18)   Which among the following is pre-defined in the standard package as one-dimensional array type comprising each element of BIT type?**

**a. Bit type  
b. Bit\_vector type  
c. Boolean type  
d. All of the above**

**ANSWER: Bit\_vector type**

**19)   In composite data type of VHDL, the record type comprises the elements of \_data types.**

**a. Same  
b. Different  
c. Both a and b  
d. None of the above**

**ANSWER: Different**

**20)   Which among the following wait statement execution causes the enclosing process to suspend and then wait for an event to occur on the signals?**

**a. Wait until Clk = ‘1’  
b. Wait on x,y,z  
c. Wait on clock until answer > 80  
d. Wait for 12 ns**

**ANSWER: Wait on x,y,z**

**21)   After an initialization phase, the simulator enters the \_\_\_\_\_\_phase.**

**a. Compilation  
b. Elaboration  
c. Execution  
d. None of the above**

**ANSWER: Execution**

**22)   An event is nothing but \_\_\_\_\_\_ target signal, which is to be updated.**

**a. Fixed  
b. Change on  
c. Both a and b  
d. None of the above**

**ANSWER: Change on**

**23)   Which among the following EDA tool is available for design simulation?**

**a. OrCAD  
b. ALDEC  
c. Simucad  
d. VIVElogic**

**ANSWER: VIVElogic**

**24)   The ‘next’ statements skip the remaining statement in the \_\_\_\_\_\_\_\_ iteration of loop and execution starts from first statement of next iteration of loop.**

**a. Previous  
b. Next  
c. Current (present)  
d. None of the above**

**ANSWER: Current (present)**

**25)   An Assert is \_\_\_\_\_\_ command.**

**a. Sequential  
b. Concurrent  
c. Both a and b  
d. None of the above**

**ANSWER: Both a and b**

**26)   Why is the use of mode buffer prohibited in the design process of synthesizer?**

**a. To avoid mixing of clock edges  
b. To prevent the occurrence of glitches & metastability  
c. Because critical path has preference in placement  
d. Because Maximum ASIC vendors fail to support mode buffer in librari**

**ANSWER: Because Maximum ASIC vendors fail to support mode buffer in libraries**

**27)   If a port is declared as buffer, then which problem is generated in hierarchical design due to mapping with port of buffer mode of other entities only?**

**a. Structural Modeling  
b. Functional Modeling  
c. Behavioral Modeling  
d. Data Flow Modeling**

**ANSWER: Structural Modeling**

**28) Sequential Statements**

**a. Can be anywhere in the statement part of an architecture.**

**b. Are always described with variables, because they need instant (sequential) value update.**

**c. neither of them**

**Answer . Neither of them**

**29) Loops**

**a) with infinite passed are not synthesizable**

**b) do not need to declare the loop identifier in the architecture declarative part**

**c) both of them.**

**Answer: Both of them**

**30) A process**

**a) can either have a sensitivity list or wait statements but not both.**

**b) with wait statements is executed until the timing conditions in the wait statements are fulfilled and retired afterwards.**

**C) Both of them**

**Answer: Can either have a sensitivity list or wait statements but not both.**